

Abstract of the Disclosure

A mechanism for assuring quality of service for a context in a digital processor has a first scheduling register dedicated to the context, the register
5 having N out of M bits set, and a first scheduler that consults the register to assign issue slots to the context. The first scheduler grants issue slots for the context by referencing the N bits in the first register, and repeats a pattern of assignments of issue slots after referencing the M bits of the first register.